Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A scan driving circuit for use in a planar display comprising an active matrix, said scan driving circuit comprising:

a first sub-circuit receiving a driving signal and outputting said driving signal to a first scan line of said active matrix via a first output terminal after a predetermined time delay; and

a second sub-circuit electrically connected to said first sub-circuit, receiving said driving signal transferred from a second output terminal of said first sub-circuit, and outputting said driving signal to a second scan line of said active matrix after said predetermined time delay,

wherein said first sub-circuit further comprises a buffer circuit electrically connected to said first output terminal and said second output terminal of said first sub-circuit, amplifying power of said driving signal, and outputting said amplified driving signal to said active matrix and said second sub-circuit via said first output terminal and said second output terminal, respectively,

said buffer comprising a unidirectional conducting device electrically connected between said first output terminal and said second output terminal.

2. (Currently Amended) The scan driving circuit according to claim 1 wherein said first sub-circuit further comprises[[:]] a shift register receiving said driving signal and outputting said driving signal after said predetermined time delay in response to a clock signal~~; and~~

~~a buffer circuit electrically connected to said shift register, said active matrix and said second sub-circuit, amplifying power of said driving signal, and outputting said amplified driving signal to said active matrix and said second sub-circuit via said first output terminal and said second output terminal, respectively~~.

3. (Currently Amended) The scan driving circuit according to claim ~~2~~ 1 wherein said first sub-circuit further comprises an electro-static discharge protection circuit electrically connected to said first output terminal of said ~~buffer circuit~~ first sub-circuit for protecting said scan driving circuit from electro-static discharge damage.

4. (Currently Amended) The scan driving circuit according to claim ~~2~~ 1 wherein said buffer circuit comprises a plurality of NOT gates arranged in series.

5. (Original) The scan driving circuit according to claim 4 wherein said buffer circuit comprises at least an NOT gate electrically connected between said first

output terminal and said second output terminal in series functioning as said unidirectional conducting device.

6. (Original) The scan driving circuit according to claim 5 wherein said NOT gates is one selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate and a CMOS NOT gate.

7. (Currently Amended) The scan driving circuit according to claim 2 wherein said second sub-circuit comprises:

a shift register electrically connected to said second output terminal of said first sub-circuit, receiving said driving signal transferred from said second output terminal of said first sub-circuit, and outputting said driving signal after said predetermined time delay in response to said clock signal; and

a buffer circuit electrically connected to said shift register, said active matrix and ~~said second~~ a third sub-circuit, amplifying power of said driving signal, and outputting said amplified driving signal to said second scan ~~lone~~ line of said active matrix via ~~said first~~ a third output terminal.

8. (Currently Amended) The scan driving circuit according to claim 7 wherein said second sub-circuit further comprises an electro-static discharge protection

circuit electrically connected to said ~~first~~ third output terminal of said ~~buffer circuit~~ second sub-circuit for protecting said scan driving circuit from electro-static discharge damage.

9. (Original) The scan driving circuit according to claim 7 wherein said buffer circuit comprises a plurality of NOT gates arranged in series.

10. (Original) The scan driving circuit according to claim 9 wherein said NOT gates is one selected from a group consisting of an NMOS NOT gate, a PMOS NOT gate and a CMOS NOT gate.

11. (Currently Amended) A scan driving circuit for driving an active matrix of a planar display, said scan driving circuit comprising a plurality of sub-circuits each in communication with one of a plurality of scan lines of said active matrix, one of said sub-circuits comprising:

a signal receiving device for receiving a driving signal from a preceding sub-circuit;

a signal amplifying device for amplifying power of said driving signal and outputting an amplified driving signal;

a unidirectional conducting device disposed downstream of said signal amplifying device for transferring said amplified driving signal to said one of said scan lines unidirectionally via a first output terminal; and

a second output terminal electrically connected to said signal amplifying device, said unidirectional conducting device and a next sub-circuit for transferring said amplified driving signal to said unidirectional conducting device and said next sub-circuit.

12. (Original) The scan driving circuit according to claim 11 wherein said signal receiving device is a shift register.

13. (Original) The scan driving circuit according to claim 11 wherein said driving signal received by said signal receiving device is transferred to said signal amplifying device after a predetermined time delay in response to a clock signal.

14. (Original) The scan driving circuit according to claim 11 wherein said signal amplifying device and said unidirectional conducting device are included in a buffer circuit.

15. (Original) The scan driving circuit according to claim 11 wherein said signal amplifying device comprises a plurality of NOT gates arranged in series, and said unidirectional conducting device comprises at least an NOT gate electrically connected between said first and said second output terminals in series.

16. (Original) The scan driving circuit according to claim 15 wherein said NOT gates are selected from NMOS NOT gates, PMOS NOT gates and CMOS NOT gates.

17. (Original) The scan driving circuit according to claim 11 further comprising an electro-static discharge protection circuit electrically connected to said one sub-circuit and said one of said scan lines for protecting said scan driving circuit from electro-static discharge damage.

18. (Currently Amended) A scan driving circuit for driving an active matrix of a planar display, said scan driving circuit comprising a plurality of sub-circuits each in communication with one of a plurality of scan lines of said active matrix, one of said sub-circuits comprising:

a signal receiving device for receiving a driving signal from a preceding sub-circuit; and

a buffer circuit comprising a signal amplifying device for amplifying power of said driving signal to output an amplified driving signal, an output terminal for transferring said amplified driving signal to a next sub-circuit, and a unidirectional conducting device for transferring said amplified driving signal to said one of said scan lines unidirectionally.

19. (Original) The scan driving circuit according to claim 18 wherein said signal receiving device is a shift register.

20. (Original) The scan driving circuit according to claim 18 wherein said driving signal received by said signal receiving device is transferred to said signal amplifying device after a predetermined time delay in response to a clock signal.